REMARKS

Amendments

Amendments to the Claims

Applicant has amended the claims to correct informalities pointed out by the Examiner. No new matter has been added as a result of these amendments

Objections

Objections to the Claims

The Examiner objected to claims 5, 7, 13-14 and 19-20 as containing informalities. Applicant has corrected the informalities in claim 5, 7, 13, 19 and 20 and respectfully requests the withdrawal of the objection. Applicant further respectfully submits that no new issues are raised by the correction of the informalities.

Rejections

Rejections under 35 U.S.C. § 102(a)

Claims 1-3, 5-10, 12-15 and 18-20

Claims 1-3, 5-10, 12-15 and 18-20 stand rejected under 35 U.S.C. § 102(a) as being anticipated by Applicant's admitted prior art (APA). Applicant respectfully submits that the APA does not disclose each and every element of the invention as claimed in claims 1-3, 5-10, 12-15 and 18-20.

In particular, the Examiner is interpreting Applicant's claimed correlation between addresses in an address set as equivalent to correlations between preceding current cache miss address as described in the Background section on page 2, lines 19-21. However, as defined by Applicant on page 4, lines 22-24 of the Detailed Description, Applicant's claimed address set and the addresses in an address set are not equivalent to the combination of preceding and current cache miss addresses used by the prior art:

> Set address correlation correlates between addresses belonging to a common address set, rather than correlating between immediately successive addresses as in prior art address-address correlators.

When an Applicant defines a claim term in the specification, the claims must be interpreted in accordance with Applicant's definition [MPEP 2111.01.]. The APA cited by the Examiner discloses creating correlations between immediately successive cache miss

addresses, and does not teach or suggest correlations between current and previous addresses within an address set as defined by Applicant. Therefore, Applicant's invention as claimed in claims 1-3, 5-10, 12-15 and 18-20 is not anticipated by the APA under 25 U.S.C. § 102(a) and Applicant respectfully requests the withdrawal of the rejection of the claims.

Rejections under 35 U.S.C. § 102(b)

Claims 1-3, 5-10, 12-15 and 18-20

Claims 1-3, 5-10, 12-15 and 18-20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Alexander et al , *Distributed Prefetch-Buffer/Cache Design for High Performance Memory Systems*. Applicant respectfully submits that Alexander does not disclose each and every element of the invention as claimed in claims1-3, 5-10, 12-15 and 18-20.

Alexander discloses a distributed cache hardware architecture combined with a particular prediction and prefetch technique that hides the latency associated with DRAM access and cycle times. The prediction and prefetch technique uses a prediction table containing addresses of memory blocks. Instead of creating a correlation between individual current and previous cache miss addresses, Alexander creates a correlation between the addresses of different memory blocks containing the current and previous miss addresses. Alexander prefetches entire memory blocks and accordingly does not need to correlate between miss addresses that are in the same memory block. Thus, Alexander does not teach or suggest correlating between addresses in the same address set as claimed by Applicant.

Therefore, Applicant respectfully submits that the invention claimed in claims 1-3, 5-10, 12-15 and 18-20 is not anticipated by Alexander under 35 U.S.C. § 102(b) and respectfully requests the withdrawal of the rejection of the claims.

Rejections under 35 U.S.C. § 102(e)

Claims 1-4, 12-15 and 17-18

Claims 1-4, 12-15 and 17-18 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,516,389 to Uchihori that has an issue date of February 4, 2003. Applicant does not admit that Uchihori is prior art and reserves the right to swear behind the reference at a later date. Nonetheless, Applicant respectfully submits that

Applicant's invention as claimed in claims 1-4, 12-15 and 17-18 is not anticipated by Uchihori.

Uchihori discloses storing disk address access history in a prefetch prediction table located on the disk drive. Uchihori does not teach or suggest that that the prefetch prediction table contains correlations between current and previous addresses in the same address set as claimed by Applicant. Therefore, Uchihori does not anticipate the invention as claimed in claims 1-4, 12-15 and 17-18 and Applicant respectfully requests the withdrawal of the rejection of the claims under 35 U.S.C. § 102(e).

SUMMARY

Claims 1-20 are currently pending. In view of the foregoing amendments and remarks, Applicant respectfully submits that the pending claims are in condition for allowance. Applicant respectfully requests reconsideration of the application and allowance of the pending claims.

If the Examiner determines the prompt allowance of these claims could be facilitated by a telephone conference, the Examiner is invited to contact Sue Holloway at (408) 720-3476.

Deposit Account Authorization

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due. Furthermore, if an extension is required, then Applicant hereby requests such extension.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR
& ZAFMAN LLP

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Sheryl S. Holloway
Attorney for Applicant
Registration No. 37,850

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-3476